16.480/552

Microprocessors II and Embedded System Design

Wednesdays, 6:30pm - 9:20pm, Location: check ISIS

Prof. Yan Luo

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This syllabus may be subject to corrections and updates.

Course Description: This three-credit course provides a continuation of the study of microprocessors begun in 16.317. Topics include CPU architecture, memory interfaces and management, coprocessor interfaces, bus concepts, bus arbitration techniques, serial I/O devices, DMA and interrupt controlled devices. Focus will be placed on the design, construction, and testing of dedicated microprocessor systems (static and real-time). Hardware limitations of the single-chip system will be investigated along with microcontrollers, programming for small systems, interfacing, and communications, validating hardware and software, microprogramming of controller chips, and design methods and testing of embedded systems. Laboratories are directly related to microprocessor functions and embedded system designs.
Prerequisite(s): 16.311 - Electronics I Laboratory, 16.317 - Microprocessors Systems Design, 16.365 - Electronics I.
Note(s): All students enrolled in 16.480/552 Microprocessors Systems Design are required to have completed prerequisites or get permission from the Instructor. It is the student who is responsible for any adverse results such as being administratively withdrawn from the class or being ineligible for tuition refund due to the enforcement of these prerequisites.
Credit Hours: 3

Course Structure:

There is a 3-hour class on Wednesday evening each week. The class will be in the format of lecture and laboratory.

Text(s):

Barry B. Brey, *Intel Microprocessors*, 8th Ed. ISBN-10: 0135026458, ISBN-13: 978-0135026458
Peter Barry and Patrick Crowley, *Modern Embedded Computing: Designing Connected, Pervasive, Media-Rich Systems*, Morgan Kaufmann; 1 edition (February 10, 2012) ,ISBN-10: 0123914906, ISBN-13: 978-0123914903

Course Objectives:

At the completion of this course, students will be able to:

1. Gain an Understanding of Embedded Systems Design.
2. Become Capable of Evaluating and Implementing Memory System Organization,Decoding, and Timing.
3. Understand Different Communication Protocols and Interfaces.
4. Become Capable of Implementing Different Memory System Architectures.
5. Understand the Interaction of Hardware and Software in Embedded Systems
6. Understand emerging embedded system design technologies

Grade Distribution:

Exam 1	20%
Exam 2	20%
Labs	60% (four labs, 15% each)
Total	100%

Note: This course is double-numbered. Students enrolled in 16.480 are graded on a different scale from those in 16.552. Generally 60% is the passing grade (D) for 16.480 students, 80% is the passing grade (B) for 16.552 students.

Course Policies:

- **General**
  - Exams are closed book, closed notes unless instructed otherwise.
  - **No makeup exams will be given unless proper documents are presented (such as doctor's notes or police reports).**
- **Labs and Reports**
  - Students are expected to work in teams of up to four people. However, **each student is expected to complete and submit his/her own lab report.** The student must clearly establish authorship of a work in the report.

    Copying reports from others is an act of **plagiarism**, which is a serious offense and **all involved parties will be penalized according to the Academic Integrity Policy**.
  - **Penalty will be applied to late turn-ins: 20% deduction per one late day.**.
- **Attendance and Absences**
  - Attendance is expected and may be taken each class.
  - Students are responsible for all missed work, regardless of the reason for absence. It is also the absentee's responsibility to get all missing notes or materials.

Academic Integrity Policy :

The university has a responsibility to promote academic honesty and integrity and to develop procedures to deal effectively with instances of academic dishonesty. Students are responsible for the honest completion and representation of their work, for the appropriate citation of sources, and for respect of others academic endeavors. Academic dishonesty is prohibited in all programs of the university.
Detailes are at http://www.uml.edu/Catalog/Undergraduate/Policies/Academic-Integrity.aspx

Tentative Course Schedule:
The weekly coverage might change as it depends on the progress of the class. However, you must check course Piazza forum for updates.
Lab reports are due at 10AM on the Friday of the week.

Week	Content	Labs Due Dates
Week 1	• Introduction to Embedded System Design • Lab tutorial: PIC microcontroller and IDE	teams formed
Week 2	• Sensors and Data Acquisition • Lab 1 released: PIC-controlled sensing	
Week 3	• Lab Session • (no lecture)	
Week 4	• Intro to x86 architecture, memory interfacing • Lab tutorial: Intel Galileo	Lab 1 due
Week 5	• Interfaces and buses • Lab 2 released : PIC+Galileo: sensor control and data acquisition	
Week 6	• Exam 1 + Lab session • (no lecture)	
Week 7	• PCI, DMA, interrupts, storage devices	Lab 2 due
Week 8	• Linux device driver (1) • Lab 3 released: Linux device driver	
Week 9	• Linux device driver (2) • Lab tutorial	
Week 10	• Lab session • (no lecture)	
Week 11	• Parallel programming and multithreading • Lab 4 released: Multithreading and networking	Lab 3 Due
Week 12	• Networking of embedded devices • demo	
Week 13	• Thursday schedule • (no class)	
Week 14	• Emerging embedded system technologies (Android, IoT, etc.)	
Week 15	• Exam 2 and lab session	Lab 4 due